

Appl. No. 09/208105
Amdt. dated Mar. 16, 2004
Reply to Office action of Oct. 27, 2003

Amendments to the Specification:

Please replace the paragraph beginning at page 7, line 11, with the following amended paragraph:

Next, a method for manufacturing the IGBT 1 will be described. The manufacturing processes similar to an ordinary IGBT are carried out until forming the source electrodes ~~regions~~ 23. In other words, the substrate 2 is formed by consecutively forming the n^+ type layer 5 on the drain layer 3 and the n^- type layer 7 thereon as shown in Fig. 4A. Thereafter, the gate oxidation layer 15 and the gate electrode 17 are formed successively as shown in Fig. 4B. Ion implantation of P-type impurities is carried out by using the gate electrode 17 as a mask. Further, N-type impurities are implanted ionically by using both [a] resist layers 81 formed on the gate oxidation layer 15 and the gate oxidation layers 17 as a mask as shown in Fig. 4C. The base region 21 with P^+ type and a pair of the source regions 23 located in the base region 21 are formed simultaneously by carrying out thermal treatment as shown in Fig. 5A.

Please replace the paragraph beginning at page 8, line 15, with the following amended paragraph:

As shown in Fig. 7B, the source ~~region~~ electrode 22 is formed by carrying out etching using a resist layer 84 being formed. As a result of the etching, the opening 25 is formed on the silicon oxidation layer 27.